AMENDMENTS TO THE CLAIMS

Upon entry of the present amendment, the status of the claims will be as is shown below. This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF THE CLAIMS

1. (Currently Amended) A cache memory which holds, for each cache entry, order data indicating an access order, and which replaces a cache entry that is oldest in the access order, the cache entry holding unit data for caching, comprising:

a modifier that modifies the order data regardless of an actual access order; and

a selector that selects, based on the modified order data, a cache entry to be replaced,

wherein said modifier attaches, to the modified order data, an oldest-order flag which indicates, when enabled, that the access order is the oldest regardless of the actual access order and which indicates that the cache entry to be replaced is written to no further,

wherein the cache entry to be replaced has, as the order data, a 1-bit order flag that indicates whether the cache entry to be replaced has been accessed since each cache entry had been reset, each cache entry being reset when a 1-bit order flag is enabled for each cache entry,

wherein said selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having the ~~an~~ oldest-order flag enabled ~~attached~~ is present, and

wherein said selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag ~~attached is not~~ unenabled is present.

2. (Previously Presented) The cache memory according to claim 1,

wherein said modifier comprises:

a specifier that specifies a cache entry that holds data which is within an address range specified by a processor; and

an oldest-orderer that causes the order data of the specified cache entry to be oldest in the access order, regardless of the actual access order.

3. (Previously Presented) The cache memory according to claim 2, wherein said specificer comprises :

a first converter that converts a starting address of the address range to a start line address that indicates a starting line within the address range when the starting address indicates a midpoint in line data;

a second converter that converts an ending address of the address range to an end line address that indicates an ending line within the address range when the ending address indicates the midpoint in the line data; and

a judger that determines whether there is a cache entry that holds data corresponding to each line address from the start line address to the end line address.

4. (Cancelled).

5. (Cancelled).

6. (Cancelled).

7. (Previously Presented) The cache memory according to claim 1,

wherein said modifier modifies the order data so that one cache entry is indicated as an

Nth cache entry in the access order, wherein

N is a number indicating one of: an oldest cache entry in the access order; a number indicating a newest cache entry in the access order; an Nth cache entry from the oldest in the access order; and an Nth cache entry from the newest cache entry in the access order.

8. (Previously Presented) The cache memory according to claim 1, wherein said modifier comprises:

an instruction detector that detects that a memory access instruction that includes a modification directive for the access order has been executed; and

a rewriter that rewrites the order data for a cache entry that is accessed due to the memory access instruction.

9. (Previously Presented) The cache memory according to claim 1, wherein said modifier comprises:

a holder that holds an address range specified by a processor;

a searcher that searches for a cache entry that holds data corresponding to the address range held in said holder; and

a rewriter that rewrites the order data so that the access order of the cache entry searched for by said searcher is an Nth cache entry in the access order.

10. (Currently Amended) A control method for controlling a cache memory which holds, in each cache entry, order data indicating an access order, and which replaces a cache entry that is oldest in the access order, the cache entry holding unit data for caching, said method comprising:

modifying the order data regardless of an actual access order; and

selecting, based on the modified order data, a cache entry to be replaced,

wherein in said modifying, an oldest-order flag is attached to the modified order data which indicates, when enabled, that the access order is the oldest regardless of the actual access order and which indicates that the cache entry to be replaced is written to no further,

wherein the cache entry to be replaced has, as the order data, a 1-bit order flag that indicates whether the cache entry to be replaced has been accessed since each cache entry had been reset, each cache entry being reset when a 1-bit order flag is enabled for each cache entry,

wherein the cache entry to be replaced is selected when a cache miss occurs and a cache entry having the ~~an~~ oldest-order flag enabled ~~attached~~ is present, and

wherein the cache entry to be replaced is selected in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag unenabled ~~attached~~ is ~~not~~ present.

11. (New) A cache memory which holds, for each cache entry, order data indicating an access order, and which replaces a cache entry that is oldest in the access order, the cache entry holding unit data for caching, comprising:

an oldest-orderer that modifies the order data regardless of an actual access order, by attaching, to the order data, an oldest-order flag which indicate, when enabled, that the access order is the oldest regardless of the actual access order and which indicates that the cache entry to be replaced is written to no further; and

a selector that selects, based on the modified order data, a cache entry to be replaced,

wherein the cache entry to be replaced has, as the order data, a 1-bit order flag that indicates whether the cache entry to be replaced has been accessed since each cache entry had

been reset, each cache entry being reset when a 1-bit order flag is enabled for each cache entry

wherein said selector selects the cache entry to be replaced when a cache miss occurs and a cache entry having the oldest-order flag enabled is present, and

wherein said selector selects the cache entry to be replaced in accordance with the order data when the 1-bit order flag indicates that the cache entry to be replaced has been accessed since each cache entry had been reset and when the cache entry having the oldest-order flag unenabled is present.